BIRZEIT UNIVERSITY
Faculty of Engineering and Technology
Electrical and Computer Engineering Department

ENCS234, Digital Systems
Date: Thursday , 09/06/2016
Time: 11:00 - 13:30
Rooms: KNH625
Total points: 100

Instructors:	Khader Mohammad	M, W	14:00 - 15:20
	Mohammed Hussein	T, R	08:00 - 09:20
	Ahmad Alsadeh	S, M, W	10:00 - 10:50
		S, M, W	13:00 - 13:50

Name:_____ **ID**:_____

Question 1: Multiple choices are worth 2 points each**. (30 points)**
(ABET Outcome a: Ability to apply mathematics, science and engineering principles.)

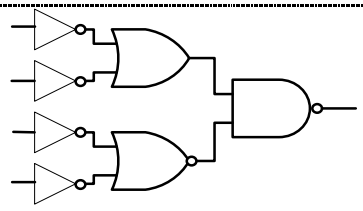
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1) Converting $(153)_{10}$ to base 8 yields which of the following results?
- a. 107
- b. 132
- c. 701
- **d. 231**

2) 10100 is the two's complement representation of:
- a. +12
- **b. -12**
- c. -20
- d. +20

3) Simplification of the Boolean expression AB + ABC + ABCD + ABCDE + ABCDEF yields which of the following results?
- a. ABCDEF
- **b. AB**
- c. AB + CD + EF
- d. A + B + C + D + E + F

4) The shown circuit can be implemented using a minimum of :
- a. 3 NAND Gates
- **b. 4 NAND Gates**
- c. 5 NAND Gates
- d. 4 NAND Gates and 1 NOR Gate



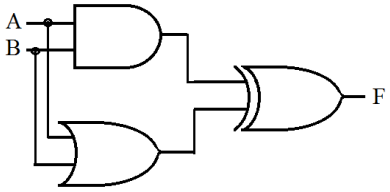
5) What is the output of the following circuit?

a. AB

b. A+B

c. A'B'+AB

d. A'B+AB'



6) Identify the function which generates the K-map shown

a. F(A,B,C) = $\sum$ (0,2,4,7)

b. **F(A,B,C) = $\sum$ (1,3,5,6)**

c. F(A,B,C) = $\sum$ (3,4,5,6)

d. F(A,B,C) = $\prod$ (1,3,5,7)

C \ AB	00	01	11	10
0	0	0	1	0
1	1	1	0	1

7) Identify the most simple Product of Sums (POS) expression which generates the K-map show

a. $F(A, B, C) = (A + C')(A + B + C)$

b. $F(A, B, C) = (A + B)(B + C')$

c. $\mathbf{F(A, B, C) = (A' + B')(A' + C)(B' + C)}$

d. $F(A, B, C) = (A' + C)(A' + B' + C)$

C \ AB	00	01	11	10
0	1	0	0	0
1	1	1	0	1

8) Identify the simplest expression from the K-map shown.

a. $F(A, B, C, D) = BC' + BCD' + AC'D'$

b. $F(A, B, C, D) = BC' + BCD' + AB'C'D'$

c. $F(A, B, C, D) = AD + BCD' + CD$

d. $\mathbf{F(A, B, C, D) = BC' + BD' + AC'D'}$

CD \ AB	00	01	11	10
00		1	1	1
01		1	1	
10				
11		1	1	

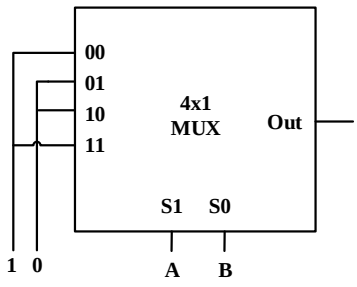
9) The circuit has the same functionality

a. **XNOR**

b. XOR

c. NAND

d. NOR



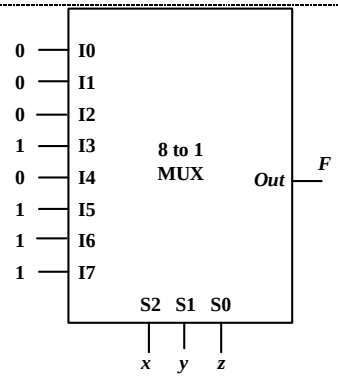
10) For the shown multiplexer, the Boolean function:

a. F = x' y + x' z + y z

b. **F = x y + x z + y z**

c. F = x y' + x z + y' z

d. F = x y + x z' + y z'



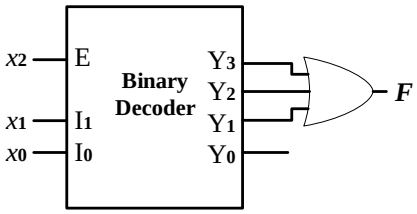
11) In the shown circuit, given *"X"* is a 3-bit binary number ($x_2x_1x_0$):

a. F = 1 when "X" is less than 4

b. **F = 1 when "X" is greater than 4**

c. F = 1 when "X" is an even number

d. F = 1 when "X" is an odd number



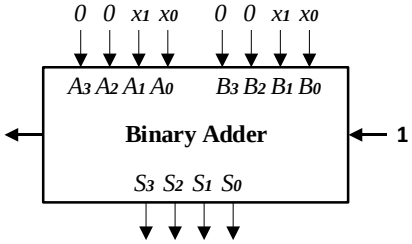
12) In the shown circuit, given *"X"* is a 2-bit binary number (x_1x_0):

a. Sum = X

b. Sum = 2 X

c. **Sum = 2 X + 1**

d. Sum = 2 X + 2



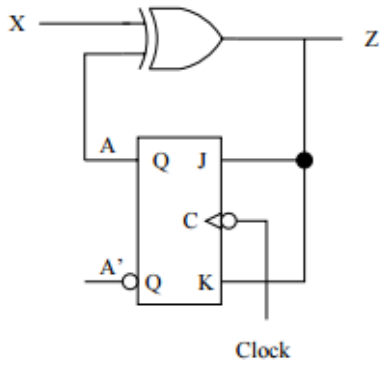
13) The sequential circuit below yields an output sequence of Z= 11011111 when you apply the input sequence X = 01101010. What is the starting state of the JK Flip-Flop?

a. A, A' = 0, 0

b. A, A' = 0,1

c. **A, A' = 1, 0**

d. A, A' = 1, 1



14) A Universal Shift Register, USR, is connected as shown. S_1 = 1, S_0 = 1 select load operation. Initially $Q_3Q_2Q_1Q_0$ = 1010.

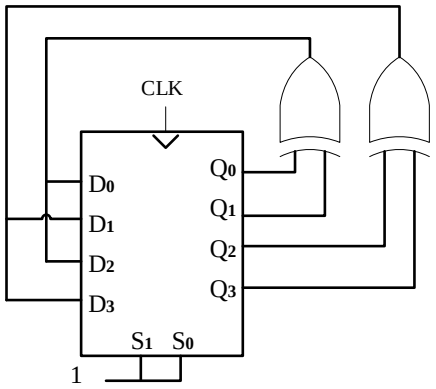
After 2 clock cycles:

a. **$Q_3Q_2Q_1Q_0$ = 0000**

b. $Q_3Q_2Q_1Q_0$ = 1111

c. $Q_3Q_2Q_1Q_0$ = 1001

d. $Q_3Q_2Q_1Q_0$ = 1010



15) For the Given State Table:

a. States A and B are equivalent

b. **States A and D are equivalent**

c. States C and D are equivalent

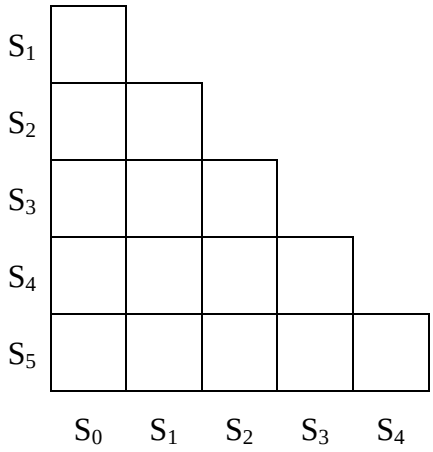
d. States C and E are equivalent

Present State	Next State		Output	
	x=0	*x=1*	*x=0*	*x=1*
A	B	D	0	1
B	A	B	1	1
C	E	A	0	0
D	B	D	0	1
E	D	C	1	0

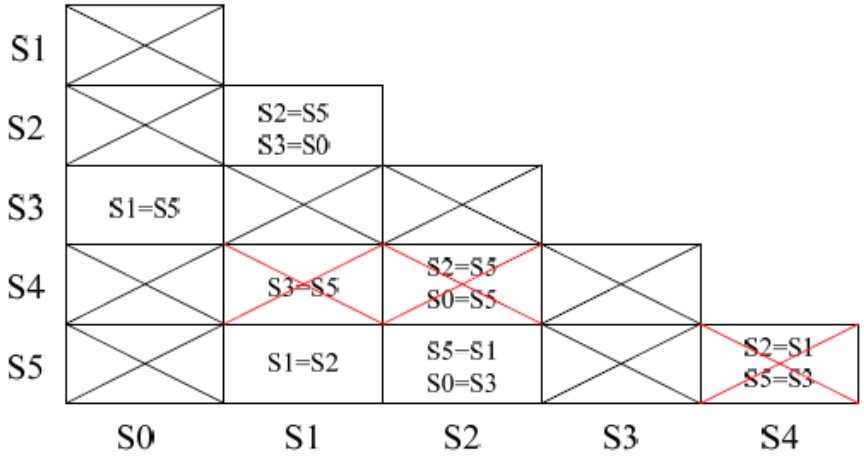
Question 2 (15 points)

A Mealy machine has one input X and one output Z. Given the following next-state table, use the **triangular table** provided below to minimize the number of states (use the implication chart method).

Present State	Next State		Output Z	
	X=0	X=1	X=0	X=1
S_0	S_4	S_1	0	1
S_1	S_2	S_3	1	0
S_2	S_5	S_0	1	0
S_3	S_4	S_5	0	1
S_4	S_2	S_5	1	0
S_5	S_1	S_3	1	0



Present state	Next state		Output Z	
	X=0	X=1	X=0	X=1
S_0	S_4	S_1	0	1
S_1	S_2	S_3	1	0
S_2	S_5	S_0	1	0
S_3	S_4	S_5	0	1
S_4	S_2	S_5	1	0
S_5	S_1	S_3	1	0



g0: {S0, S3}

g1: {S1, S2, S5}

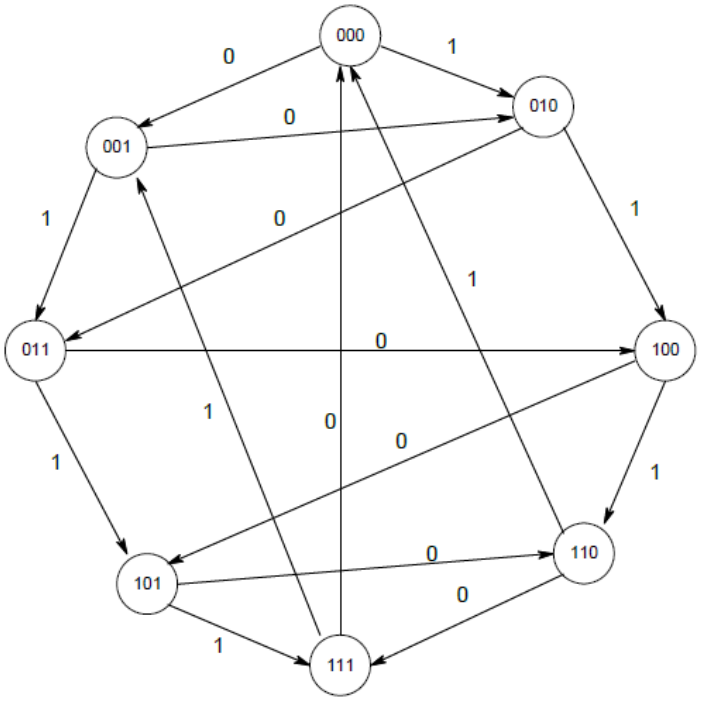
g2: {S4}

g3:

Present state	Next state		Output Z	
	X=0	X=1	X=0	X=1
g0	g2	g1	0	1
g1	g1	g0	1	0
g2	g1	g1	1	0

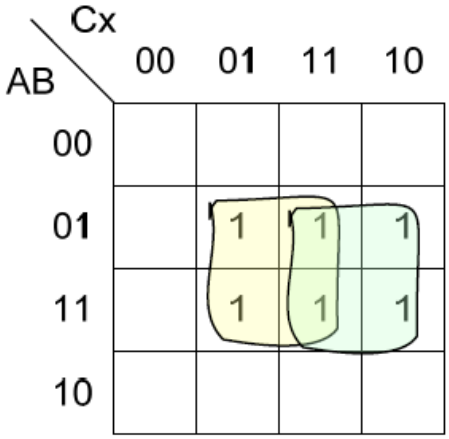
<u>Question 3</u> (20 points) (ABET Outcome c: Ability to design a system, component, or process to meet desired needs.)

Design the sequential circuit specified by the state diagram of Fig. Q2b using T flip-flops. (**20 points**)

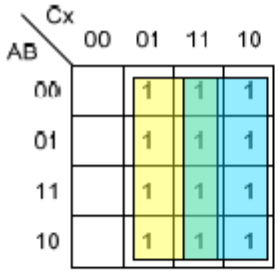


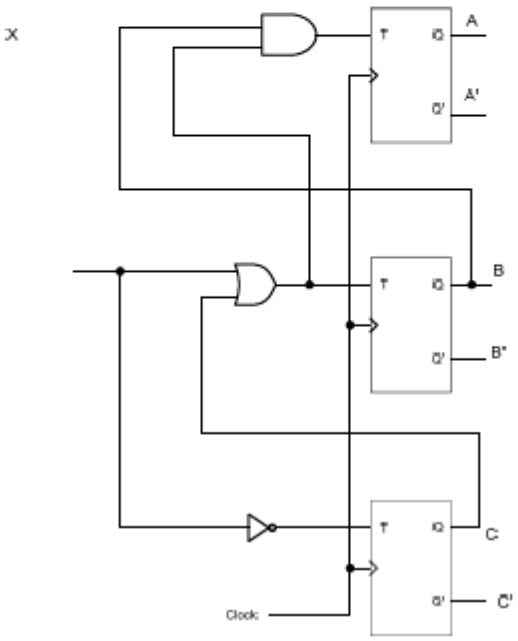
Present State			Input	Next State			Flip-flop Inputs		
A	B	C	x	A	B	C	T_A	T_B	T_C
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	0
0	0	1	0	0	1	0	0	1	1
0	0	1	1	0	1	1	0	1	0
0	1	0	0	0	1	1	0	0	1
0	1	0	1	1	0	0	1	1	0
0	1	1	0	1	0	0	1	1	1
0	1	1	1	1	0	1	1	1	0
1	0	0	0	1	0	1	0	0	1
1	0	0	1	1	1	0	0	1	0
1	0	1	0	1	1	0	0	1	1
1	0	1	1	1	1	1	0	1	0
1	1	0	0	1	1	1	0	0	1
1	1	0	1	0	0	0	1	1	0
1	1	1	0	0	0	0	1	1	1
1	1	1	1	0	0	1	1	1	0

$T_C = x'$



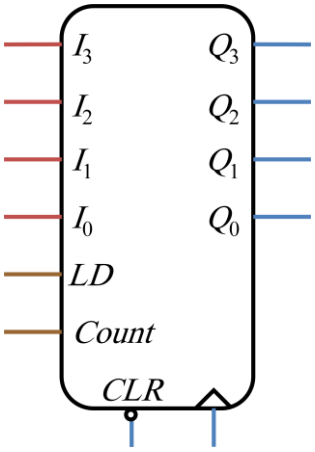
$T_A = Bx + BC = B(x + C)$


Cx
AB
00
01
11
10
00
01
11
10
1
T_A=x+C

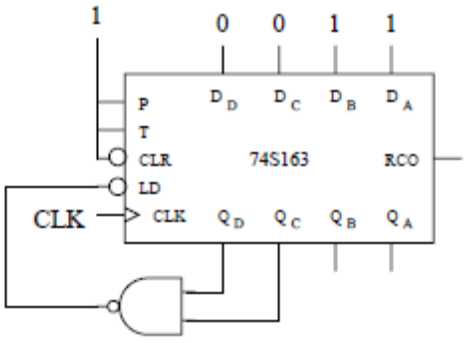

X
T
Q
Q'
A
A'
B
B'
C
C'
Clock

Question 4 (20 points)

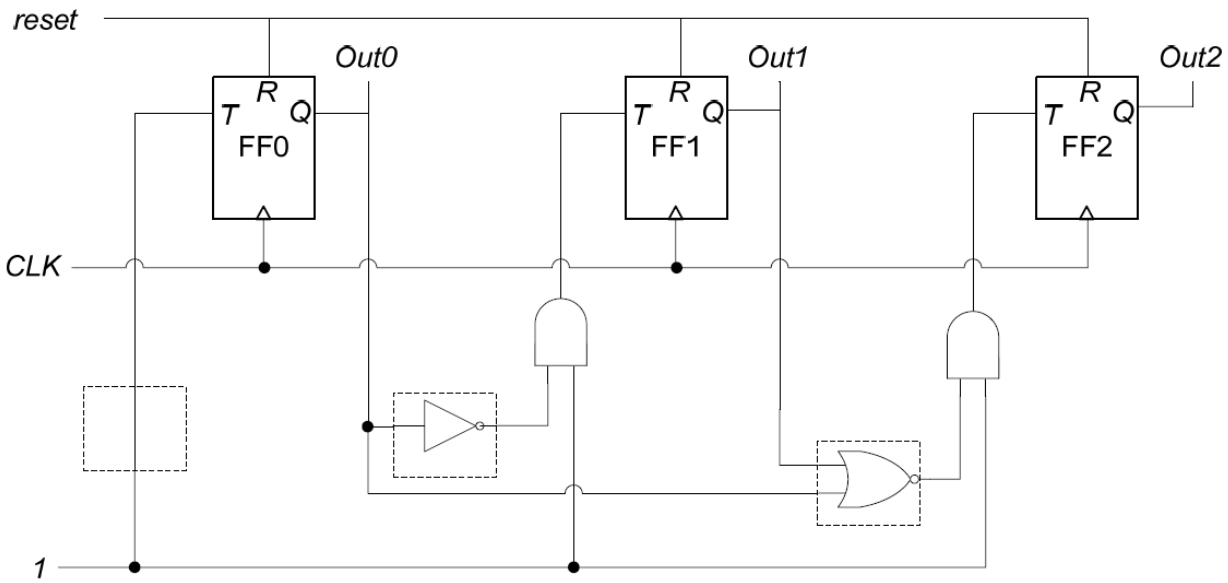
a) Using the counter shown below and logic gates design a counter that counts in the sequence 3,4, 5, 6, 7, 8, 9, 10, 11, 12, 3, ... Connect all unused inputs. The counter may cycle through several unwanted states before settling into the final count sequence. Q_3 is the most significant bit of the counter output. (**10 points**)



Function Table for the Counter				
CLR	***CLK***	***LD***	***Count***	**Function**
0	x	x	x	Clear to 0
1	↑	1	x	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change



a) An incomplete schematic of a **down-counter** is shown below. This design uses **T flip-flops** as the internal storage. You are asked to finish up this design by filling in all the boxes. Each box can only contain a **direct wire** or exactly one gate which must belong to the cell library **{AND, OR, NAND, NOR, XOR, XNOR, inverter}**. (**10 points**)



Question 5 (15 points) (ABET Outcome e: Ability to identify, formulate and solve engineering problems.)

a. Write a Verilog description for the MUX2x1 (**5 points**)
b. Write a Verilog description for the DFF (**5 points**)
c. Structurally build the Circuit in the figure (**5 points**)